REMARKS

The Examiner rejected claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21, 22 and 30-36 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of and Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

The Examiner rejected claims 3 and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 1 and 12 above, and further in view of Moslehi *et al.* (5,296,385; hereinafter "Moslehi").

The Examiner rejected claims 6-9 and 17-20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 5 and 16 above, and further in view of Sugino (5,121,705).

Applicants respectfully traverse the § 103 rejections with the following arguments.

35 U.S.C. § 103(a)

Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21, 22, and 30-36

Claims 1, 2, 4, 5, 10, 11, 12, 13, 15, 16, 21, 22, and 30-36 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Koze (4,687,682) in view of Kiyosumi *et al.* (4,603,059; hereinafter, "Kiyosumi").

Applicants respectfully contend that claims 1 and 12 as amended is not unpatentable over Koze in view of Kiyosumi, because Koze in view of Kiyosumi does not teach or suggest each and every feature of claims 1 and 12.

For example, Koze in view of Kiyosumi does not teach or suggest the feature of "wherein the first semiconductor wafer is located **directly adjacent** to the second semiconductor wafer such that **no additional semiconductor wafers** of said plurality of semiconductor wafers are located **between** a **topside** of the first semiconductor wafer and a **backside** of a portion of the second semiconductor wafer" (emphasis added).

The Examiner argues: "Koze discloses a method of fabricating semiconductor wafer 100 (Fig. 1), comprising: providing a plurality of semiconductor wafers 100, wherein the plurality of wafers comprises a first semiconductor wafer and a second semiconductor wafer, and wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer (note in Fig. 1, any of wafers 100 could be chosen as the first and second wafers)".

In response, Applicants respectfully contend that Koze in Fig. 1, does not teach or suggest placing a first semiconductor wafer **directly adjacent** to a second semiconductor wafer such that there are **not** any other semiconductor wafers located **between** a **topside** of the first semiconductor wafer and a **backside** of the second semiconductor wafer as taught by Applicant's

claims 1 and 12. In contrast, Koze teaches in col. 3, lines 1-3, " Referring to FIG. 1, silicon wafers (100 are placed by pairs into wafer boats (101), so that the **active** face of one wafer **contacts** the **active** face of another ". Therefore, Applicants contend that Koze teaches an **active** face of one wafer **contacting** an **active** face on another wafer and therefore the Koze invention **cannot** exclude an additional semiconductor wafer located between a topside (i.e., active side) of a first semiconductor wafer and a backside (a non-active side) of a second semiconductor wafer as taught by Applicant's claims 1 and 12.

The Examiner further alleges in response to the Office Action response filed on November 29, 2005 (i.e., in response to the Office Action mailed on September 1, 2005) that "Koze discloses the wafers 100 are placed by pairs into wafer boats 101, i.e., a plurality of wafer pairs are placed in each boat. Therefore, even if the active faces of two wafers are in contact with each other, one wafer of a first pair can be readily interpreted as the first semiconductor wafer in claims 1 and 12 and another wafer of a second pair would be the second semiconductor wafer of the claimed invention, wherein the front sides of each of said one wafer and said another wafer face the same direction. In other words, in Koze's disclosure, a plurality of pairs of wafers are provided in each boat such that one wafer from each of two pairs of wafers can be readily chosen to be the first and second semiconductor wafers of the claimed invention".

In response, Applicants respectfully contend that the Examiner's argument of "even if the active faces of two wafers are in contact with each other, one wafer of a first pair can be readily interpreted as the first semiconductor wafer in claims 1 and 12 and another wafer of a second pair would be the second semiconductor wafer of the claimed invention" further illustrates that Koze teaches an **extra wafer** located **between** a topside of a first semiconductor wafer and a backside

of a second semiconductor wafer. Therefore, Applicants contend that Koze does not teach a first semiconductor wafer **directly adjacent** to a second semiconductor wafer such that there are **not** any other semiconductor wafers located **between** a **topside** of the first semiconductor wafer and a **backside** of the second semiconductor wafer as taught by Applicant's claims 1 and 12.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 12 are not unpatentable over Koze in view of Kiyosumi, and that claims 1 and 12 are in condition for allowance. Since claims 2, 4, 5, 10, 11, and 30-32 depend from claim 1 and claims 13, 15, 16, 21, 22, and 33-36 depend from claim 12, Applicants contend that claims 2, 4, 5, 10, 11, 13, 15, 16, 21, 22, and 30-36 are likewise in condition for allowance.

Claims 3 and 14

Claims 3 and 14 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 1 and 12 above, and further in view of Moslehi *et al.* (5,296,385; hereinafter "Moslehi").

In response, Applicants contend that since claim 3 depends from claim 1 and claim 14 depends from claim 12 which Applicants have argued *supra* to not be unpatentable over Koze in view of Kiyosumi under 35 U.S.C. §103(a), Applicants maintain that claims 3 and 14 are likewise not unpatentable over Koze (in view of Kiyosumi) and further in view of Moslehi under 35 U.S.C. §103(a).

Claims 6-9 and 17-20

Claims 6-9 and 17-20 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Koze (in view of Kiyosumi) as applied to claims 5 and 16 above, and further in view of Sugino (5,121,705).

In response, Applicants contend that since claims 6-9 depend from claim 1 and claims 17-20 depend from claim 12 which Applicants have argued *supra* to not be unpatentable over Koze in view of Kiyosumi under 35 U.S.C. §103(a), Applicants maintain that claims 6-9 and 17-20 are likewise not unpatentable over Koze (in view of Kiyosumi) and further in view of Sugino under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

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